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Ritenour

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(54) **LATERAL SEMICONDUCTOR DEVICE WITH VERTICAL BREAKDOWN REGION**

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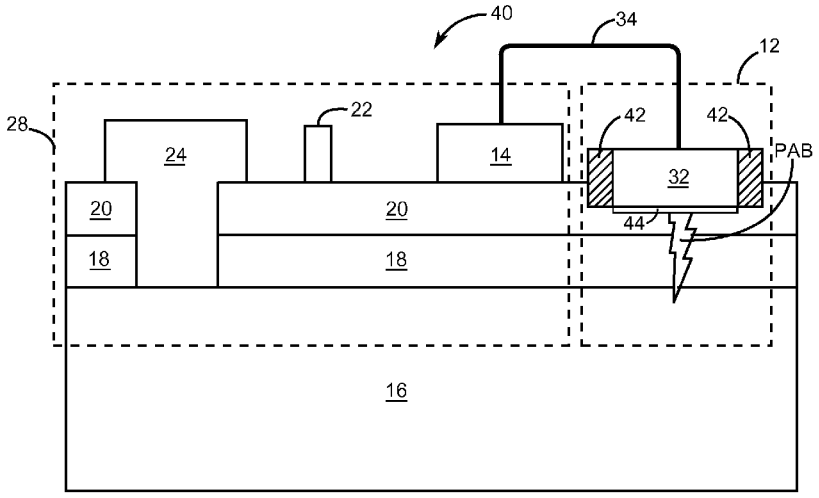
(57) **ABSTRACT**

A lateral semiconductor device having a vertical region for providing a protective avalanche breakdown (PAB) is disclosed. The lateral semiconductor device has a lateral structure that includes a conductive substrate, semi-insulating layer(s) disposed on the conductive substrate, device layer(s) disposed on the semi-insulating layer(s), along with a source electrode and a drain electrode disposed on the device layer(s). The vertical region is separated from the source electrode by a lateral region wherein the vertical region has a relatively lower breakdown voltage level than a relatively higher breakdown voltage level of the lateral region for providing the PAB within the vertical region to prevent a potentially damaging breakdown of the lateral region. The vertical region is structured to be more rugged than the lateral region and thus will not be damaged by a PAB event.

18 Claims, 2 Drawing Sheets



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Notice of Allowance for U.S. Appl. No. 13/910,202, mailed May 14, 2015, 9 pages.
Notice of Allowance for U.S. Appl. No. 13/974,488, mailed May 29, 2015, 9 pages.
Corrected/Supplemental Notice of Allowability for U.S. Appl. No. 13/957,689, mailed May 20, 2015, 3 pages.
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* cited by examiner

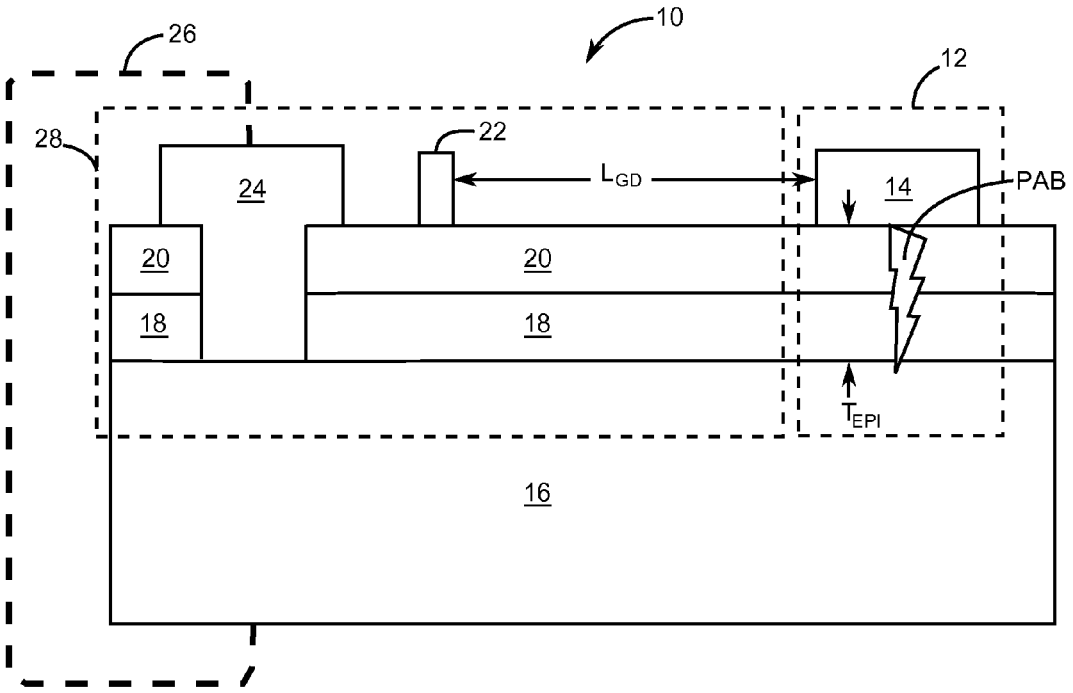
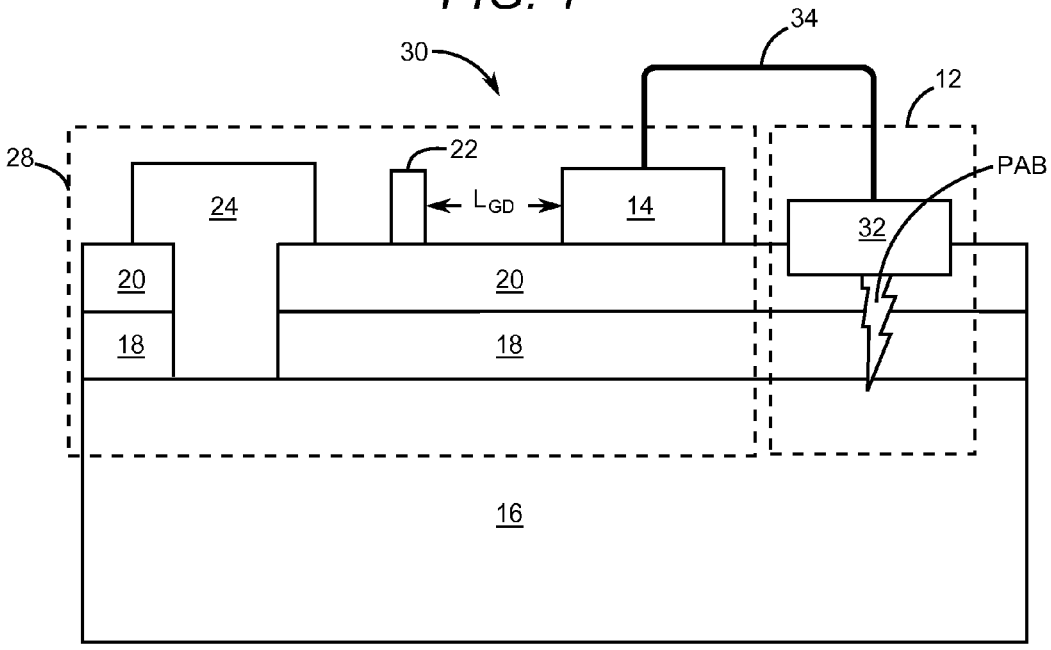

26
10
12
28
22
24
L_{GD}
14
PAB
20
20
18
18
T_{EPI}
16

FIG. 1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30
12
28
22
24
L_{GD}
14
32
PAB
20
20
18
18
16

FIG. 2

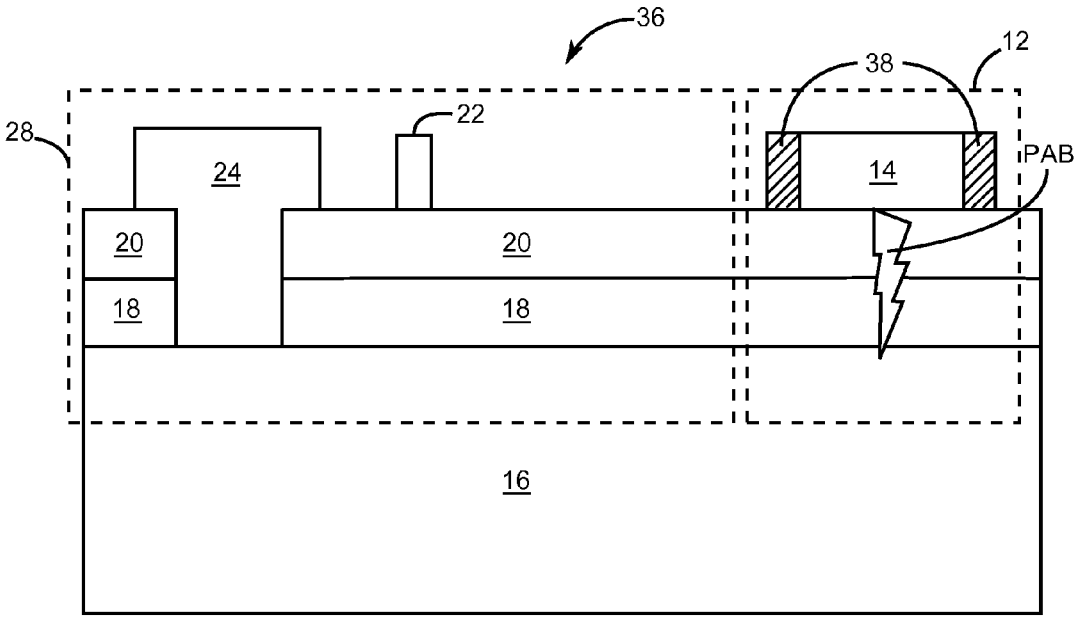
36
38
12
28
22
24
14
PAB
20
20
18
18
16

FIG. 3

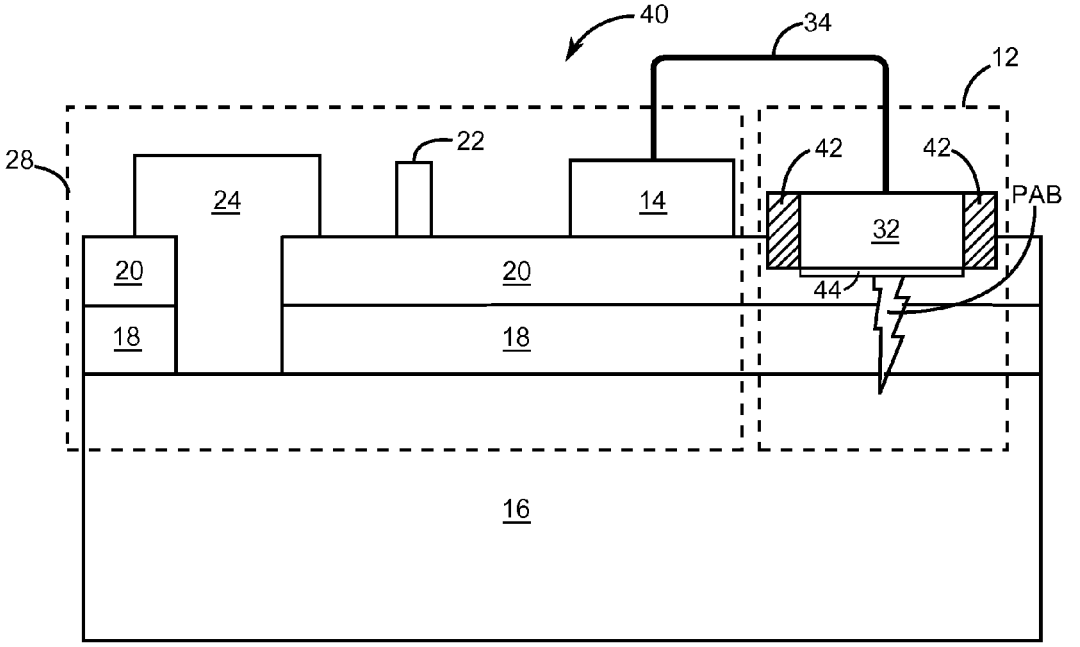
40
34
12
28
22
42
42
24
14
PAB
32
20
20
44
18
18
16

FIG. 4

LATERAL SEMICONDUCTOR DEVICE WITH VERTICAL BREAKDOWN REGION

RELATED APPLICATIONS

This application claims the benefit of U.S. provisional patent application No. 61/693,487, filed Aug. 27, 2012, the disclosure of which is incorporated herein by reference in its entirety.

FIELD OF THE DISCLOSURE

The present disclosure relates to electronic devices that include overvoltage and current surge protection.

BACKGROUND

Gallium nitride (GaN) is commonly cited as a superior material for high-voltage power devices due to its wide bandgap and associated high electric field required for avalanche breakdown. Ideal bulk GaN crystals have critical fields in excess of 3,000,000 V per centimeter. However, during operation of a lateral semiconductor device such as a GaN high electron mobility transistor (HEMT) a generally two dimensional electric field is concentrated at the corners of a gate and/or field plates. As a result, high electric fields can occur in dielectrics around the gate and/or field plates. Moreover, in practice, a high electric field needed for avalanche breakdown is lowered by non-idealities that are present within the structure of a GaN device. During high-voltage operation of a GaN device, electrical breakdown will typically occur at defects and/or at locations with a concentrated electric field. An example of such a breakdown location is a corner of a Schottky gate. An ideal structure comprising a bulk crystal such as silicon carbide (SiC) or GaN will avalanche uniformly in a high electric field region. As a result, avalanche energy is distributed uniformly, which greatly enhances the survivability of a device made up of an ideal bulk crystal. For example, vertical p-n junctions fabricated in SiC homoepitaxial layers demonstrate avalanche breakdown ruggedness. However, breakdown in defective GaN layers will typically occur at defects within defective GaN layers. A resulting high energy density typically causes irreversible damage to a device that includes defective GaN layers.

Another factor impacting breakdown ruggedness is the nature of the metal semiconductor contacts that carry a breakdown current. Previous work with SiC Schottky diodes has demonstrated that Schottky contacts can be degraded by avalanche current. In response to this problem, junction barrier Schottky diodes have been developed to urge avalanche breakdown to occur across a bulk p-n junction with ohmic contacts rather than Schottky contacts. Thus, the breakdown ruggedness of GaN HEMTs may be limited by breakdown events in highly localized areas within a semiconductor due to crystal defects and/or electric field concentration. Moreover, the breakdown ruggedness of GaN HEMTs may be limited by an electrical breakdown of adjacent dielectric layers and/or high current flow through the Schottky gate electrode during breakdown events. Thus, there is a need to provide overvoltage protection for a lateral semiconductor device to ensure that the lateral semiconductor device handles a typically destructive breakdown voltage without being damaged.

SUMMARY

A lateral semiconductor device having a vertical region for providing a protective avalanche breakdown (PAB) is disclosed. The lateral semiconductor device has a lateral structure that includes a conductive substrate, semi-insulating layer(s) disposed on the conductive substrate, device layer(s) disposed on the semi-insulating layer(s), along with a source electrode and a drain electrode disposed on the device layer(s). The vertical region is separated from the source electrode by a lateral region wherein the vertical region has a relatively lower breakdown voltage level than a relatively higher breakdown voltage level of the lateral region for providing the PAB within the vertical region to prevent a potentially damaging breakdown of the lateral region. The vertical region is structured to be more rugged than the lateral region and thus will not be damaged by a PAB event. As a result, the lateral semiconductor device of the present disclosure has an advantage of surviving potentially damaging overvoltage and current surges.

Those skilled in the art will appreciate the scope of the disclosure and realize additional aspects thereof after reading the following detailed description in association with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

FIG. **1** is sectional view of a lateral transistor having a vertical region for protective avalanche breakdown between a drain electrode and a conductive substrate.

FIG. **2** is a sectional view of a lateral transistor wherein the vertical region includes an avalanche electrode coupled to the drain electrode and the conductive substrate.

FIG. **3** is a sectional view of a lateral transistor wherein the drain electrode includes an edge termination and is located within the vertical region.

FIG. **4** is a sectional view of a lateral transistor wherein the drain electrode is coupled to the avalanche electrode that includes an edge termination.

DETAILED DESCRIPTION

The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the disclosure and illustrate the best mode of practicing the disclosure. Upon reading the following description in light of the accompanying drawings, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

It will be understood that when an element such as a layer, region, or substrate is referred to as being "over," "on," "in," or extending "onto" another element, it can be directly over, directly on, directly in, or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over," "directly on," "directly in," or extending "directly onto" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

The present disclosure describes embodiments of a lateral semiconductor device having a vertical region for providing a protective avalanche breakdown (PAB) that enhances the voltage breakdown ruggedness of the lateral semiconductor device. The vertical region provides a relatively lower breakdown voltage than a lateral region of the lateral semiconductor device. As such, the vertical region prevents a voltage breakdown from occurring in the lateral region of the lateral semiconductor device.

FIG. **1** is a first embodiment of a lateral semiconductor device in the form of lateral transistor **10** having a vertical region **12** for protective avalanche breakdown between a drain electrode **14** and a conductive substrate **16**. For the purpose of this disclosure, a PAB is represented by a lightning bolt symbol. A semi-insulating layer(s) **18** and a device layer(s) **20** are disposed between the drain electrode **14** and the conductive substrate **16** with the drain electrode **14** being disposed onto the device layer(s) **20**. A gate electrode **22** and a source electrode **24** are also disposed on the device layer(s) **20**. However, the source electrode **24** is coupled to the conductive substrate **16** either internally or optionally by an external connection **26**, which is shown using a thick dashed line in FIG. **1**. The vertical region **12** has a relatively lower breakdown voltage in comparison to a relatively larger breakdown voltage of a lateral region **28**. As a result, voltage breakdown is prevented from occurring within the lateral region **28**.

The relatively lower breakdown voltage is achieved in this embodiment by adjusting a thickness T_{EPI} of epitaxial layers making up the semi-insulating layer(s) **18** and the device layer(s) **20** inside the vertical region **12** to be relatively less than a minimum lateral distance L_{GD} between the drain electrode **14** and gate electrode **22**. Moreover, a lateral distance L_{GD} between the drain electrode **14** and the gate electrode **22** substantially influences the breakdown voltage of the lateral region **28**. Moreover, other causes that influence the breakdown voltage of the vertical region **12** and the breakdown voltage of the lateral region **28** might not be related. As such, no assumption is made that the T_{EPI} should be less than the L_{GD} in all circumstances. However, the T_{EPI} is less that the L_{GD} in typical circumstances. In any case, adjustments to the T_{EPI} relative to the L_{GD} must ensure that the breakdown voltage of the vertical region **12** is consistently less than the breakdown voltage of the lateral region **28**. Preferably, a PAB should occur in the vertical region **12** just before a voltage breakdown of the lateral region **28**. Yet, as alluded to above, a margin between the PAB and the voltage breakdown of the lateral region **28** must be maintained to ensure the PAB occurs before the voltage breakdown of the lateral region **28**.

FIG. **2** is a lateral transistor **30** wherein the vertical region **12** includes an avalanche electrode **32** coupled to the drain electrode **14**. In this embodiment, the avalanche electrode **32** is located within the vertical region **12** and is partially embedded in the device layer(s) **20**. Moreover, the drain electrode **14** is disposed on the device layer(s) **20** at a location outside of the vertical region **12** and inside the lateral region **28**. The drain electrode **14** is coupled to the avalanche electrode **32** via a conductor **34**.

FIG. **3** is a sectional view of a lateral transistor **36** wherein the drain electrode **14** includes an edge termination **38** and is located within the vertical region **12**. The edge termination **38** reduces a two-dimensional electric field about the edge of the drain electrode **14**, thereby making a PAB that occurs within the vertical region **12** more uniform.

FIG. **4** is a sectional view of a lateral transistor **40** wherein the avalanche electrode **32** includes an edge termination **42** for reducing a two-dimensional electric field that typically forms about the avalanche electrode **32**. In this embodiment, the avalanche electrode **32** is located within the vertical region **12** and is partially embedded in the device layer(s) **20**. Moreover, the drain electrode **14** is disposed on the device layer(s) **20** at a location outside of the vertical region **12** and inside of the lateral region **28**. The drain electrode **14** is coupled to the avalanche electrode **32** via the conductor **34**.

In at least one of the above embodiments, at least a portion of the vertical region **12** between the drain electrode **14** or avalanche electrode **32** and the conductive substrate **16** is doped to form a p-n junction **44** between the drain electrode **14** and the conductive substrate **16**. The p-n junction **44** is a relatively rugged semiconductor structure that allows a PAB event to be non-destructive. In at least one embodiment, the p-n junction **44** comprises at least a portion of the drain electrode **14** of FIGS. **1** and **3**, or the avalanche electrode **32** of FIGS. **2** and **4**. Moreover, in at least one embodiment, at least a portion of the drain electrode **14** or the avalanche electrode **32** in contact with the device layer(s) **20** is an ohmic contact. In at least one other embodiment, at least a portion of the drain electrode **14** or the avalanche electrode **32** in contact with the device layer(s) **20** is a Schottky contact. The conductive substrate **16** can be, but is not limited to, silicon carbide (SiC), silicon (Si), gallium nitride (GaN), and zinc oxide (ZnO). In one embodiment, a bulk resistivity for the conductive substrate **16** ranges from around about 100 ohm-cm to around about 10 ohm-cm. In another embodiment, a bulk resistivity for the conductive substrate **16** ranges from around about 10 ohm-cm to around about 0.01 ohm-cm.

It is to be understood that the structures and techniques of the present disclosure are extendable to semiconductor devices other than transistors. For example, a lateral diode having a drain electrode that is an anode and a source electrode that is a cathode can be fabricated to include the vertical region for providing a PAB.

Those skilled in the art will recognize improvements and modifications to the embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

What is claimed is:

1. A lateral semiconductor device comprising:

a lateral structure comprising:

a conductive substrate;

at least one semi-insulating layer disposed on the conductive substrate;

at least one device layer disposed on the at least one semi-insulating layer;

a source electrode disposed on the at least one device layer;

a drain electrode disposed on the at least one device layer;

a vertical region that includes the drain electrode and at least a portion of the conductive substrate and that is separated from the source electrode by a lateral region wherein a breakdown voltage level for a protective avalanche breakdown (PAB) of the vertical region is lower than a breakdown voltage level of the lateral region; and

an edge termination integral with the drain electrode.

2. The lateral semiconductor device of claim 1 wherein epitaxial layers making up the at least one semi-insulating layer and the at least one device layer have a thickness that is less than a minimum lateral distance between the drain electrode and a gate electrode disposed on the at least one device layer, thereby lowering the breakdown voltage level for a PAB of the vertical region relative to the breakdown voltage level of the lateral region.

3. The lateral semiconductor device of claim 1 wherein at least a portion of the vertical region between the drain electrode and the conductive substrate is doped to form a p-n junction between the drain electrode and the conductive substrate.

4. The lateral semiconductor device of claim 3 wherein the p-n junction comprises at least a portion of the drain electrode.

5. The lateral semiconductor device of claim 1 further including an avalanche electrode disposed on the at least one device layer within the vertical region and coupled to the drain electrode, wherein the drain electrode is within the lateral region.

6. The lateral semiconductor device of claim 5 further including an edge termination integral with the avalanche electrode.

7. The lateral semiconductor device of claim 5 wherein the avalanche electrode is at least partially embedded within the at least one device layer.

8. The lateral semiconductor device of claim 5 wherein at least a portion of the vertical region between the drain electrode and the conductive substrate is a p-n junction.

9. The lateral semiconductor device of claim 8 wherein the p-n junction comprises at least a portion of the avalanche electrode.

10. The lateral semiconductor device of claim 5 wherein at least a portion of the avalanche electrode is an ohmic contact.

11. The lateral semiconductor device of claim 5 wherein at least a portion of the avalanche electrode is a Schottky contact.

12. The lateral semiconductor device of claim 1 wherein at least one portion of the drain electrode is an ohmic contact.

13. The lateral semiconductor device of claim 1 wherein at least a portion of the drain electrode is a Schottky contact.

14. The lateral semiconductor device of claim 1 wherein the conductive substrate is silicon carbide (SiC).

15. The lateral semiconductor device of claim 1 wherein the conductive substrate is gallium nitride (GaN).

16. The lateral semiconductor device of claim 1 wherein the conductive substrate is zinc oxide (ZnO).

17. The lateral semiconductor device of claim 1 wherein a bulk resistivity of the conductive substrate ranges from around about 100 ohm-cm to around about 10 ohm-cm.

18. The lateral semiconductor device of claim 1 wherein a bulk resistivity of the conductive substrate ranges from around about 10 ohm-cm to around about 0.01 ohm-cm.

* * * * *